

Notice of References Cited

Application/Control No.

09/388,766

Applicant(s)/Patent Under
Reexamination
SHIH ET AL.

Examiner

Ayal I Sharon

Art Unit

2123

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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,680,332	10-1997	Raimi et al.	703/13
	B	US-6,175,946	01-2001	Ly et al.	716/4
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	IEEE Std. 1164-1993. IEEE Standard Multivalued Logic System for VHDL Model Interoperability (Std_logic_1164). (c) 1993.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
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